## Features

Atmel's ProChip Designer v4.0 with the Mentor Graphics<sup>®</sup> Software Update seamlessly integrates the following software components into one Integrated Development Environment (IDE):

- Precision<sup>®</sup> RTL Synthesis VHDL and Verilog<sup>®</sup> synthesis supports from Mentor Graphics
- ModelSim  $^{\ensuremath{\text{e}}}$  VHDL and Verilog simulation supports from Mentor Graphics
- PeakFPGA<sup>™</sup> VHDL synthesis and simulation support from Altium<sup>®</sup>
- Protel<sup>®</sup> 99SE Schematic and CUPL<sup>®</sup> design entry, synthesis and simulation supports from Altium
- FIT15xx Fitters for the ATF15xx CPLDs from Atmel
- HDL Planner VHDL and Verilog design entry and text editing support from Atmel
- ATMEL ISP JTAG In-System programming (ISP) support from Atmel

# Description

Atmel's ProChip Designer is a fully featured EDA software suite incorporating state-ofthe-art synthesis and simulation tools from Mentor Graphics and Altium with Atmel's user-friendly interface/design navigator and powerful fitter technologies. The combination of these tools will enable CPLD designers to achieve the highest possible logic utilization from the Atmel ATF15xxAS/ASL/ASV/ASVL/BE series CPLDs (Complex Programmable Logic Devices) with Logic Doubling<sup>®</sup> features.

Through all of the software components available within the ProChip Designer Software Suite, the following features are supported:

- Design Entry & Synthesis
  - VHDL
  - Verilog
  - CUPL
  - Schematic
- Simulation
  - VHDL functional and timing simulation
  - Verilog functional and timing simulation
  - CUPL functional simulation
- Device
  - ATF15xxBE 1.8V ultra-low-power CPLD
  - ATF15xxAS/ASL 5.0V standard and low-power CPLD
  - ATF15xxASV/ASVL 3.3V standard and low-power CPLD
- Programming
  - JTAG ISP

# **Software Suite Components**

The software components within the ProChip Designer Software Suite are divided into two groups. These two software groups, their contents, license terms and ordering code are described in Table 1 in detail.





ProChip Designer<sup>®</sup> Software Suite Overview



Software	Content	License Term	
ProChip Designer v4.0	Evaluation Edition		
	ProChip Designer v4.0	Free	
	30-day Trial version of Altium PeakFPGA	<b>F 60 1 1 1 1</b>	
	30-day Trial version of Altium Protel99SE	Free 30-day trial period	
	Licensed Edition		
	ProChip Designer v4.0	Free	
	Licensed version of Altium PeakFPGA	Permanent license	
	Licensed version of Altium Protel99SE	[P/N: ATDS1500PC]	
Mentor Graphics Software Update	ProChip 4.0 Software Patch	Free	
	MGC Precision RTL Synthesis	Free 6-month evaluation license	
	MGC ModelSim	1-year license [P/N: ATDS15xxKSW1]	
	License Configuration Utility	Free	
	Atmel ISP	Free	

#### Table 1. ProChip Designer Software Suite Contents and License Terms

Note: Atmel's software tools are supported on Microsoft<sup>®</sup> Windows<sup>®</sup> operating systems. The details of the operating system supports for other vendors' tools can be obtained from the third-party tool vendors' websites or documentation.

For the ProChip Designer v4.0 Evaluation Edition, it comes with the 30-day Trial version of Altium PeakFPGA and Protel 99SE. A license is not needed to install the trial version software. However, they can be installed onto a PC only once. When the trial period expires, users can purchase the Licensed Edition of ProChip Designer v4.0 from Atmel using the ordering code [ATDS1500PC]. Upon the purchase, a ProChip Designer v4.0 Software CD along with the 16-digit Access Code (permanent license) will be mailed. Users can then follow the installation instructions to uninstall the Evaluation Edition software and install the Licensed Edition software.

The ProChip Designer v4.0 Evaluation Edition is available on the ProChip Designer v4.0 Software CD and the Atmel website at www.atmel.com/dyn/products/tools\_card.asp?tool\_id=2756.

After successfully installing ProChip Designer v4.0 (Evaluation or Licensed Edition), the Mentor Graphics Software Update should be installed by following the installation instructions provided with the update. This update adds the support for the ATF15xxBE, Mentor Graphics Precision and ModelSim, latest fitters, and latest Atmel CPLD ISP software into the ProChip Designer v4.0 Software Suite.

To use Precision or ModelSim, a FLEXLM<sup>®</sup> license file from Atmel is required. A 6-month evaluation license can be obtained from Atmel by registering online at www.atmel.com/products/pld/forms/reg\_license.asp. Atmel also offers annual (1-year) licenses for Precision/ModelSim, which can be purchased using the ordering code [ATDS15xxKSW1]. Upon the purchase, a ProChip Designer v4.0 Software CD along with a Serial Number will be mailed. Users can then request for the annual license from Atmel online at the URL shown above with the Serial Number provided. Note: The license terms for Altium PeakFPGA/Protel 99SE and Mentor Graphics Precision/ModelSim are independent of each other. Therefore, even after the 30-day Trial period for the Altum tools has expired, Precision and ModelSim can continue to be used until the license period for them expires. Similarly, Protel 99SE and PeakFPGA can continue to be used even after the license period for Precision/ModelSim has expired.

## **Software Design Flow**

The ProChip Designer v4.0 IDE is shown in Figure 1. The Design Flow chart on the right provides push-button access to all the stages of a design cycle. Description of the features for each design flow stage is described in Table 2.

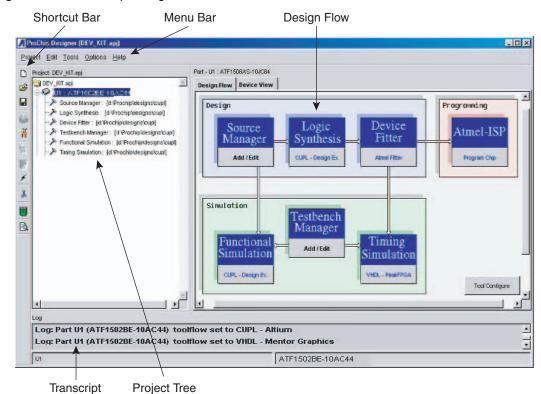


Figure 1. ProChip Designer v4.0 IDE





Table 2. Description of Design	1 Flow Stages
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Design Flow Stage	Description	
Source Manager	To specify the new or existing design file(s). Launches the appropriate design entry tool for editing based on the selected tool-flow.	
Logic Synthesis	To synthesize the design file(s) to generate the appropriate netlist file.	
Device Fitter	To fit the netlist into the target device with the user selected fitter options.	
Testbench Manager	To specify the new or existing testbench file(s). Launches the appropriate testbench entry tool for editing based on the selected tool-flow.	
Functional Simulation	To perform functional simulation on the design file(s).	
Timing Simulation	To perform timing simulation on the output netlist generated by the fitter after fitting.	
Atmel ISP	To program the target ATF15xx CPLD through JTAG-ISP.	

For details on how to use ProChip, refer to the ProChip Designer Help File, tutorials, and Online Resources. These resources are available under the ProChip Help menu.

## **Technical Support**

Submit questions online at: http://www.atmel.com/dyn/products/support.asp FAQ: http://www.atmel.com/dyn/products/tech\_support.asp?Faq=y

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## **Atmel Corporation**

2325 Orchard Parkway San Jose, CA 95131, USA Tel: 1(408) 441-0311 Fax: 1(408) 487-2600

## **Regional Headquarters**

#### Europe

Atmel Sarl Route des Arsenaux 41 Case Postale 80 CH-1705 Fribourg Switzerland Tel: (41) 26-426-5555 Fax: (41) 26-426-5500

### Asia

Room 1219 Chinachem Golden Plaza 77 Mody Road Tsimshatsui East Kowloon Hong Kong Tel: (852) 2721-9778 Fax: (852) 2722-1369

#### Japan

9F, Tonetsu Shinkawa Bldg. 1-24-8 Shinkawa Chuo-ku, Tokyo 104-0033 Japan Tel: (81) 3-3523-3551 Fax: (81) 3-3523-7581

## **Atmel Operations**

*Memory* 2325 Orchard Parkway San Jose, CA 95131, USA Tel: 1(408) 441-0311 Fax: 1(408) 436-4314

### Microcontrollers

2325 Orchard Parkway San Jose, CA 95131, USA Tel: 1(408) 441-0311 Fax: 1(408) 436-4314

La Chantrerie BP 70602 44306 Nantes Cedex 3, France Tel: (33) 2-40-18-18-18 Fax: (33) 2-40-18-19-60

#### ASIC/ASSP/Smart Cards

Zone Industrielle 13106 Rousset Cedex, France Tel: (33) 4-42-53-60-00 Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd. Colorado Springs, CO 80906, USA Tel: 1(719) 576-3300 Fax: 1(719) 540-1759

Scottish Enterprise Technology Park Maxwell Building East Kilbride G75 0QR, Scotland Tel: (44) 1355-803-000 Fax: (44) 1355-242-743

#### **RF**/Automotive

Theresienstrasse 2 Postfach 3535 74025 Heilbronn, Germany Tel: (49) 71-31-67-0 Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd. Colorado Springs, CO 80906, USA Tel: 1(719) 576-3300 Fax: 1(719) 540-1759

## Biometrics/Imaging/Hi-Rel MPU/

High-Speed Converters/RF Datacom Avenue de Rochepleine BP 123 38521 Saint-Egreve Cedex, France Tel: (33) 4-76-58-30-00 Fax: (33) 4-76-58-34-80

*Literature Requests* www.atmel.com/literature

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